ABSTRACT OF THE DISCLOSURE

A gate is formed on a device formation region of a semiconductor substrate, and source and drain regions are formed in the device formation region of the semiconductor substrate adjacent respective sides of the gate. The gate is formed to include a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer. An etch stop layer is formed over the source region, the drain region and the sidewall spacers of the gate to obtain an intermediate structure, and a planarized first interlayer insulating film is formed over a surface of the intermediate structure. The first insulating layer is dry etched until the etch stop layer over the source region, the drain region and the sidewall spacers is exposed to form self-aligned contact holes in the first interlayer insulating over the source region and the drain region, respectively. The etch stop layer is then wet etched to remove the etch stop layer over the source region, the drain region and the sidewall spacers, and respective contact pads are formed by filling the self-aligned contact holes with conductive polysilicon.